## REMARKS

The Applicants respectfully request reconsideration and allowance of claims 1-18 in view of the above amendments and the following arguments.

### I. THE TELEPHONE INTERVIEW

The Applicants appreciate the telephone interview conducted between Examiner Tat and the undersigned attorney on August 8, 2007. In the telephone interview, the participants discussed how the Office Action applied the Puri patent (described further below) to the present claims. The undersigned attorney noted that the reference did not address logic synthesis and did not disclose the elements set out in the present claims as described further below. The participants also discussed the references to the "single dynamic logic circuit," "intermediate circuit," and "final circuit" in the claims and how these elements are shown in Figures 3, 5, and 6, respectively. Finally, the participants discussed the Section 101 rejections and the significance of the resulting circuits produced according to the claimed methods. No agreement was reached as to the patentability of the claims.

### II. THE AMENDMENTS

Independent claim 13 has been amended to require that the improvement includes performing logic synthesis for the predetermined logical operation to produce an intermediate circuit. Support for this amendment can be found in the original specification for the present application at page 8, lines 16-18.

No new matter has been added by the amendment to claim 13. Claims 1 through 18 remain pending in the case.

III. THE CLAIMS ARE DIRECTED TO STATUTORY SUBJECT MATTER

The Office Action rejected claims 1, 8, and 13 under 35 U.S.C. §101 for being directed to non-statutory subject matter. Specifically, the outstanding Office Action indicates that claims 1, 8, and 13 are each directed to an abstract idea that is not tied to a technological art, environment, or machine which would result in a practical application producing a concrete result. The Applicants respectfully traverse this rejection as to claims 1 and 8. Claim 13 is amended above to clarify that the claimed improvement produces a concrete result, and is thus clearly directed to statutory subject matter as amended.

Claim 1 is directed to a method of designing a logic circuit to provide a predetermined logical operation and includes the following steps:

(a) defining a logic synthesis block comprising a single dynamic logic circuit;
(b) performing logic synthesis for the predetermined logical operation to produce an intermediate circuit, the logic synthesis being performed utilizing a synthesis library constrained to the logic synthesis block;
(c) eliminating unused devices in the intermediate circuit to produce a final circuit; and
(d) sizing the devices in the final circuit.

This claim language clearly specifies a process, one of the four statutory categories of patentable inventions defined under 35 U.S.C. §101. Given that the claim specifies a process, the issue then is whether the claimed process is merely a law of nature, natural phenomenon, or abstract idea, that is, one of the three categories of subject matter that has been found unpatentable. *Diamond v. Diehr*, 209 USPQ 1, 7 (1981). A claimed invention is considered statutory when it falls within one of the four statutory categories of patentable subject matter and produces a useful and concrete or tangible result. *See State Street Bank & Trust Co. v. Signature Financial Group Inc.*, 47 USPQ2d 1596 (Fed. Cir. 1998). In this case claim 1 starts with a specific type of logic synthesis block and concludes with sizing devices in a final circuit. This final circuit with the

various sized electronic devices represents a useful, concrete, and tangible result required for a claim to define statutory subject matter. Thus claim 1 does not merely recite an abstract idea, law of nature, or natural phenomenon.

In view of the useful, concrete, and tangible result produced by the method set out in claim 1, the Applicants submit that claim 1 is clearly directed to statutory subject matter. Therefore, the Applicants request that the Section 101 rejection of claim 1 be withdrawn.

Claim 8 is directed to a method of synthesizing a logic circuit to provide a predetermined logical operation and includes the following steps:

(a) defining a logic synthesis block comprising a single dynamic logic circuit; and
(b) performing logic synthesis for the predetermined logical operation to produce an intermediate circuit, the logic synthesis utilizing a synthesis library constrained to the single dynamic logic circuit comprising the logic synthesis block.

This claim language also clearly specifies a process. Considering that the claim defines a process, the issue then is whether the process produces a useful and concrete or tangible result as discussed above. In this case claim 8 requires method steps that included defining a logic synthesis block comprising a specific circuit type, and performing logic synthesis utilizing a synthesis library constrained to that defined logic synthesis block. The method of claim 8 ultimately results in an intermediate circuit. This intermediate circuit represents a useful, concrete, and tangible result required for a claim to define statutory subject matter. Thus claim 8 does not merely recite an abstract idea, law of nature, or natural phenomenon.

In view of the useful, concrete, and tangible result produced by the method set out in claim 8, the Applicants submit that claim 8 is clearly directed to statutory subject matter and not merely to an abstract idea. Therefore, the Applicants request that the Section 101 rejection of claim 8 be withdrawn.

Claim 13 as amended above is directed to a method of utilizing a logic synthesis tool and predefined logic circuit library to provide a logic implementation for a predetermined logical operation. The improvement set out in the claim requires the following steps:

(a) defining a logic synthesis block comprising a single dynamic logic circuit; and
(b) in performing logic synthesis for the predetermined logical operation to produce an intermediate circuit, constraining the logic synthesis tool to the logic synthesis block.

Similarly to claim 8, this claim language specifies a process and also requires producing an intermediate circuit. This intermediate circuit represents a useful, concrete, and tangible result required for a claim to define statutory subject matter. Thus claim 13 does not merely recite an abstract idea, law of nature, or natural phenomenon.

In view of the useful, concrete, and tangible result produced by the method set out in claim 13, the Applicants submit that claim 13 is directed to statutory subject matter and not merely to an abstract idea. Therefore, the Applicants believe that the Section 101 rejection of claim 13 should be withdrawn.

## IV. THE CLAIMS ARE NOT ANTICIPATED BY PURI

The current Office Action rejected claims 1-18 under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 6,018,621 to Puri et al. ("Puri" or the "Puri patent"). The Applicants submit that Puri does not anticipate these claims because Puri does not disclose all of the limitations required by claims 1-18.

The present application includes three independent claims, claims 1, 8, and 13. Due to the nature of the claims, claim 8 will be addressed first in the comments below.

Independent Claim 8

Independent claim 8 is directed to a method of synthesizing a logic circuit to provide a predetermined logical operation and requires the following limitations:

(a) defining a logic synthesis block comprising a single dynamic logic circuit; and
(b) performing logic synthesis for the predetermined logical operation to produce an intermediate circuit, **the logic synthesis utilizing a synthesis library constrained to the single dynamic logic circuit** comprising the logic synthesis block.

A specific example of a circuit design method implementing the limitations required by claim 8 can be found starting on page 7, line 6 of the specification of the present application. This example defines the logic synthesis block as a four high and four wide dynamic AND/OR circuit ("4A4O"). (See p. 7, line 9 - p. 8, line 13). An intermediate circuit is produced by the logic synthesis tool using the 4A4O circuit in the synthesis library. (See Figure 4 and p. 8, line 14 - p. 9, line 7). The intermediate circuit includes the number of 4A4O circuits needed to implement the predetermined logical function. (See Figure 5 and p. 11, line 17 - p. 12, line 8). The intermediate circuit does not include any other circuit besides 4A4O circuits because the synthesis library utilized during logic synthesis was constrained to using only a single dynamic logic circuit, the 4A4O circuit. Thus, as can be seen from not only the plain language of the claim, but also from the above example, the logic synthesis block of claim 8 comprises simply a single dynamic logic circuit, such as a 4A4O circuit, and the logic synthesis required at element (b) of claim 8 is performed using just this single dynamic logic circuit in the synthesis library.

The Puri patent discloses a logic design technique which starts with an initial network of logic gates and then moves invert logic gates (i.e. NOT gates) to the network inputs and outputs. The disclosed technique converts logic gates in the network to AND, OR, or NOT gates, identifies a region in the network, and selects between moving the NOT gates towards the network inputs or the network output within the identified region.

Puri, however, does not disclose defining a logic synthesis block comprising a single dynamic logic circuit as required by claim 8. Puri also does not perform a logic synthesis at all and certainly does not disclose constraining a synthesis library to a single dynamic logic circuit as required by claim 8. In fact, the Puri patent does not even mention a circuit "synthesis library." Since Puri does not disclose a synthesis library, it is impossible for Puri to disclose constraining a synthesis library to a single dynamic logic circuit as required by claim 8.

Because the Puri patent does not disclose all of the limitations required by claim 8, the Applicants submit that claim 8 is not anticipated by Puri. Claim 8 should therefore be in condition for allowance along with its respective dependent claims, claims 9-12.

Claim 1

Claim 1 requires limitations similar to those required by claim 8. In particular, claim 1 requires **performing logic synthesis where the synthesis library is constrained to a single dynamic logic circuit**. Thus, the arguments presented above with respect to claim 8 apply with equal force to claim 1.

In addition, claim 1 requires eliminating unused devices in the intermediate circuit to produce a final circuit. Puri, however, does not disclose any unused devices after logic synthesis takes place nor does Puri disclose the removal of unused devices from an intermediate circuit. Therefore, since Puri does not disclose all of the limitations required by claim 1, the Applicants submit that Puri does not anticipate claim 1.

For these reasons, the Applicants submit that claim 1 is not anticipated by the Puri patent and is entitled to allowance along with its respective dependent claims, claims 2-7.

Independent Claim 13

Claim 13 is directed to a circuit design method utilizing a logic synthesis tool and predefined logic circuit library to provide a logic implementation for a predetermined logical

operation. The improvements required by claim 13 include defining a logic synthesis block comprising **a single dynamic logic circuit** and **constraining the logic synthesis tool to the logic synthesis block in performing logic synthesis**. As discussed above with respect to claims 1 and 8, the Puri patent does not disclose these limitations. Therefore, since Puri does not disclose all of the limitations required by claim 13, the Applicants submit that Puri cannot anticipate claim 13.

For these reasons, the Applicants submit that claim 13 is not anticipated by the Puri patent and is entitled to allowance along with its respective dependent claims, claims 14-18.

## V. CONCLUSION

For all of the above reasons, the Applicants respectfully request reconsideration and allowance of claims 1-18.

If any issue remains as to the allowability of these claims, or if a further conference might expedite allowance of the claims, the Examiner is asked to telephone the undersigned attorney prior to issuing a further action in this case.

Respectfully submitted,

The Culbertson Group

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By: _____

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